A Fast Simulator for the Analysis of Sub-Threshold Thermal Noise Transients

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ABSTRACT

The gate length of CMOS transistors is continuing to shrink down to the sub-10nm region and operating voltages are moving toward near-threshold and even sub-threshold values. With this trend, the number of electrons responsible for the total charge of a CMOS node is greatly reduced. As a consequence, thermal fluctuations that shift a gate from its equilibrium point may no longer have a negligible impact on circuit reliability. Time-domain analysis helps understand how transient faults affect a circuit and can guide designers in producing noise-resistant circuitry. However, modeling thermal noise in the time-domain is computationally very costly. Moreover, small fluctuations in electron occupation introduce time-varying biasing point fluctuations, increasing the modeling complexity. To address these challenges, this paper introduces a new approach to modeling thermal noise directly in the time domain by developing a series of stochastic differential equations (SDE) to model various transient effects in the presence of thermal noise. In comparisons to SPICE-based simulations, our approach can provide 3 orders of magnitude speedup in simulation time, with comparable accuracy. This simulation framework is especially valuable for detecting rare events that could translate into fault-inducing noise transients. While it is computationally infeasible to use SPICE to detect such rare events due to thermal noise, we introduce a new iterative approach that allows detecting 6σ events in a matter of a few hours.

1. INTRODUCTION

A major advantage of CMOS digital circuits is their relatively high signal-to-noise ratio, making them resilient to various sources of error. Even so, their error resiliency began to be challenged by the appearance of single-event upsets (SEU) due to radiation noise. Initially, SEUs were observed exclusively in memory elements and as a result much research has been targeted at error rate analysis and fault tolerance techniques specifically in SRAMs and latches [3, 2, 27, 8]. Combinational logic, on the other hand, is inherently more robust to these noise phenomena since a noise-generated glitch would have to propagate to the primary outputs and be latched to generate the wrong logic value.

The probability of any glitch or single-event transient (SET) manifesting itself as an actual fault depends on three factors: logical masking, electrical masking and latching-window masking. The degree of logical masking depends on the topology of the circuit. The ability of electrical or latching-window masking to decrease the error probability is linked to the operating voltage and feature size of the technology node in which the circuits are manufactured. In particular, transistor downscaling leads to a reduction of the node capacitance of a CMOS gate, which translates to a lower critical charge for each logic gate. Additionally, voltage scaling translates to reduced switching thresholds, which increases the probability of a glitch propagating from one stage to the next. Finally, modern pipelined designs take advantage of several pipeline stages with reduced logic depth between registers as a way to increase throughput, making glitches more likely to propagate to the primary outputs. Therefore, technology and voltage scaling have had an increasingly negative impact on noise resiliency of CMOS circuits and the design of noise-tolerant combinatorial circuits has been the focus of a number of works [1, 11, 14, 15, 18, 20, 25].

Sub-45nm technologies have brought about additional challenges to circuit reliability. Random Telegraph Signal (RTS) noise has drawn considerable attention in the past few years as a major contributor to reduced reliability of both sequential and combinational CMOS circuits. Several works have targeted the modeling of this noise source, *e.g* [12, 24, 26]. In particular, the work of Mahmutoglu *et al.* [12] and Wirth *et al.* [24] have shown the importance of taking into account time-varying biasing conditions for the correct estimation of RTS noise characteristics.

There has been an increasing interest in extremely low-power circuits, (e.g., using environmental energy harvesting for the anticipated Internet-of-Things) which would require sub-threshold circuits operated at $V_{DD} < 300$ mV. Indeed, as transistor sizes scale down below 10nm and tighter power budgets move operating voltages to near-threshold or sub-threshold values, the number of electrons charging the output node of a CMOS gate may be reduced down to only a few hundred, further compromising noise immunity. In particular, thermally-induced fluctuations, which move a gate away from its equilibrium point, will have to be considered as a fundamental reliability limiting factor. While it has been studied for years with regard to its influence on analog circuits, it is not clear how thermal noise could generate

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SET in CMOS logic.

Time-domain noise analysis offers a detailed description of the dynamic response of a circuit in the presence of noise and may be used as a guide in designing noise-immune circuitry. The state-of-the-art time-domain thermal noise simulators are based on SPICE. However, SPICE-based simulators are generally computationally very costly, especially if the goal is to observe rare fault-inducing noise transients.

Accurate modeling of thermal noise in sub-threshold circuits requires a careful choice of the proper probability distribution in order to match the physical behavior of these circuits. Thermal noise has commonly been modeled using additive white Gaussian noise (AWGN), where the voltage fluctuations follow a Gaussian distribution with zero mean and fixed standard deviation. However, when the total charge at the output of a CMOS gate is very low, even fluctuations of a few electrons can bring substantial changes to the operating point of the transistors, implying a nonlinear behavior that requires adopting time varying parameters to compute the noise. Moreover, it has been shown that thermal fluctuations in circuits operating in the sub-threshold regime follow a Poissonian rather than Gaussian distribution [19].

Given these challenges, in this paper we present a novel framework for simulating thermal noise effect directly in the time domain that is both physically accurate and computationally affordable. Specifically, in this paper we make the following contributions:

- We develop a series of stochastic differential equations (SDE) to model the transient behavior of any CMOS logic gate in the presence of thermal noise. The final value of the output voltage of any gate can be determined from the solution of the SDEs.
- We show that the SDE formulation is flexible and robust, allowing various transient effects, such as overshoot and undershoot, to be easily included in the model. This feature is especially important for accurately estimating propagation delay.
- By modeling the noise as part of the SDE, we avoid the standard two-step simulation process that requires first computing the noiseless solution and then injecting noise as an additive source.
- In comparison to SPICE-based simulations, we show that our simulator can provide more than 3 orders of magnitude speedup in runtime, with comparable accuracy.
- We provide a methodology for reducing the computational time required to detect rare events that could translate into fault-inducing noise transients.

The reminder of this paper is organized as follows: Section 2 provides an overview of related work. In Section 3, we present the derivation of the SDEs used for our circuit time-domain modeling. In Section 4 we describe the implementation of our simulator as well as the methodology used for fast detection of thermally-induced SET. We report simulation results in Section 5 and provide concluding remarks in Section 6.

2. BACKGROUND AND RELATED WORK

In recent years, there have been several efforts to address the design of thermal-noise-tolerant circuit architectures [5, 6, 13, 16]. All these works modeled the thermal noise by scaling the noise standard deviation up to a value that would allow a SET to be observed more easily in the logic circuits. While this approach does allow for some means of evaluating various circuit designs for noise robustness, the noise itself was ill-defined. In fact, while increasing the noise amplitude to a high value, such as 60 mV RMS, allows for a fast detection of fault-inducing events, these events do not reflect the transient nature of the real signals. Instead, the goal in this paper is to develop a simulation framework that allows for the fast detection of physically accurate thermal noise transients. More specifically, our approach is to develop a stochastic representation of noise fluctuations for a device operated in the sub-threshold region.

Note that thermal noise for transistors in sub-threshold operation follows statistics that are fundamentally different from those used in classical above-threshold circuits. It has been shown that for transistors in sub-threshold operation, electron fluctuations can be described using a two-sided Poisson process whose rates can be derived from the forward and reverse components of the transistors' drain current [19]. For transistors biased in sub-threshold, this current is given by:

$$I_D = I_0 \exp\Big(\frac{qV_{gs}}{mkT}\Big) \exp\Big(\frac{qV_{ds}\lambda_D}{kT}\Big)\Big[1 - \exp\Big(-\frac{qV_{ds}}{kT}\Big)\Big] \quad (1)$$

where λ_D is the DIBL parameter [22] and m and I_0 are technology-dependent factors. The rates of the two Poisson processes are directly related to the forward and reverse current components from Equation 1. The charging and discharging rates can be extracted directly from the sub-threshold current in terms of forward and reverse electron flow. For a NMOS transistor we can derive the rates expressed in terms of number of electrons per picosecond as:

$$\mu_n = \frac{I_0}{q} \exp\Big(\frac{qV_{ds}\lambda_D}{kT}\Big) \exp\Big(\frac{qV_{gs}}{mkT}\Big) \times 10^{-12} \quad (2)$$

$$\lambda_n = \mu_n \exp\Big(\frac{-qV_{ds}}{kT}\Big) \quad (3)$$

The extension of this model to the inverter gate can be easily constructed considering that the sum of two or more independent Poisson processes is still a Poisson process with a rate given by the sum of the original processes [10]. As an example, consider the inverter in Figure 1.

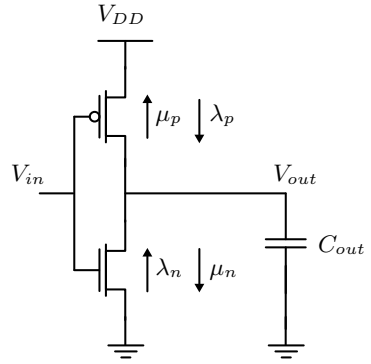

Figure 1: Inverter rates for NMOS and PMOS transistors.

Here we have adopted the convention of labeling the rates associated with the current components flowing in the output node, *i.e.* charging the output capacitance, with λ and

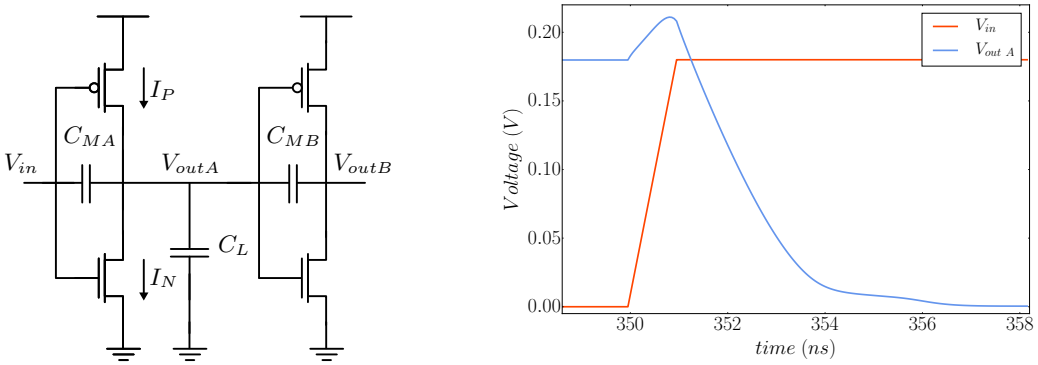

Figure 2: (a) Two inverters connected in series, and (b) the transient response at node V_{outA} to an input step function at V_{in}.

the rates for the opposing discharging process as μ. The rates for the charging/discharging processes can be summed together and the original four processes can be reduced to two cumulative opposing Poisson processes with rates $\lambda_{inv} = \lambda_n + \lambda_p$ and $\mu_{inv} = \mu_n + \mu_p$. In our formulation, we extend this simplification to any CMOS gate, regardless of the complexity of the circuit, by combining the rates of all the transistors connected to the output node.

The two-sided Poisson model has been used in [7] to create a probabilistic framework with the goal of estimating the failure rate due to thermal noise. The framework used predicted data from the ITRS to model a cross–coupled inverter in the $10nm$ technology node and it was used to investigate the failure-in-time (FIT) due to thermal noise as a function of other parameters such as fabrication process, V_{DD}, and temperature variations. Our work differs from [7] in two ways; we aim to describe the dynamic response of the circuits to voltage transients generated by thermal noise and, while doing so, we extend the study to more complex circuit architectures with multiple logic gates.

In our prior work [4], we proposed using the Ornstein–Uhlenbeck (OU) process [23] to capture the time–varying nature of the noise. However, the OU process requires additional computational complexity in order to model transient behaviors such as overshoot and undershoot effects. In fact, the OU-based solution requires a two-step simulation approach in which we first generate the noise samples, in the form of current pulses, and then we inject the resulting noise trace at the output of the noise gate in the equivalent SPICE netlist. Moreover, the simulator presented in [4] does not go beyond individual CMOS gates. Instead, we present here a different approach which models the net current at the gate's output and therefore allows us to model the circuit's behavior without the aid of additional SPICE simulations.

In the following section we present the derivation of the nodal SDEs used by our simulator for computing the output voltage of CMOS logic gates.

3. NOISE-DRIVEN SIMULATION

Consider the circuit in Figure 2(a) with transient response of the voltage at node V_{outA} shown in Figure 2(b). The overshoot shown at the beginning of the transition is caused by the input/output coupling through the Miller capacitance, C_{MA}, while the tail toward the end of the transition is due to feedback coupling through the Miller capacitance of the second stage C_{MB}. Note that this "heavy tail" is only noticeable in transient analysis for sub-threshold circuits, due to increased propagation delay.

These two effects can be modeled by considering Kirchoff's current law at the output node of the first inverter. The equilibrium state at V_{outA} when the node charge is not subject to any noise can be expressed as:

$$\frac{dV_{outA}}{dt}C_L = \frac{d\left(V_{in} - V_{outA}\right)}{dt}C_{MA} + I_P - I_N + \frac{d\left(V_{outB} - V_{outA}\right)}{dt}C_{MB}$$

The same equation can be modified to express the thermal fluctuations in the output node charge as well. For each transistor in the circuit, we express the net charge as two competing Poisson processes as described in Section 2. The MOS currents then become random variables that can be expressed in the following general form:

$$I_P - I_N = \frac{d\left(\left(X_{ch} - X_{dis}\right) \times q\right)}{dt} \tag{4}$$

where $X_{ch} \sim Poiss\left(\lambda_p + \lambda_n\right)$ and $X_{dis} \sim Poiss\left(\mu_p + \mu_n\right)$.

Kirchoff's equation can then be rewritten as:

$$\frac{dV_{outA}}{dt}C_L = \frac{d\left(V_{in} - V_{outA}\right)}{dt}C_{MA} + \frac{d\left(\left(X_{ch} - X_{dis}\right) \times q\right)}{dt} + \frac{d\left(V_{outB} - V_{outA}\right)}{dt}C_{MB} \tag{5}$$

This SDE can be used to model the state of the inverter in the presence of noise. Note that for circuits operated in sub-threshold with a total voltage swing of a few hundred mV, we can consider the transistor capacitances to be constant. Under this assumption, the solution of the SDE leads to a discrete-time iterative function that expresses the value of the output voltage in the time domain:

$$V_{outA}\left[t\right] = V_{outA}\left[t-1\right] + \left(V_{in}\left[t\right] - V_{in}\left[t-1\right]\right)\frac{C_{MA}}{C_{tot}} + \left(V_{outB}\left[t\right] - V_{outB}\left[t-1\right]\right)\frac{C_{MB}}{C_{tot}} + \frac{\left(\left(X_{ch} - X_{dis}\right) \times q\right)}{C_{tot}} \tag{6}$$

The expression given in Equation 6 represents the core of our simulator. Its uniqueness lies in the fact that it is a noise-driven simulator. In contrast to other simulators that compute the stable solution and then add noise in the analysis, our formulation allows us to directly characterize the state of a CMOS circuit in the presence of thermal noise. As a result, we can greatly speed up the simulation time

without sacrificing the accuracy of the results. Using an approach similar to [4], we can compute X_{ch} and X_{dis} for arbitrarily complex gates. For the NAND shown in Figure 3, we can define $X_{ch} \sim Poiss\left(\lambda_{p1} + \lambda_{p2} + \lambda_n\right)$ and $X_{dis} \sim Poiss\left(\mu_{p1} + \mu_{p2} + \mu_n\right)$. Notice that the contribution of the bottom NMOS transistor to the pull-down transition rate comes from setting the voltage V_x, which determines the biasing point of the transistor connected to the output node.

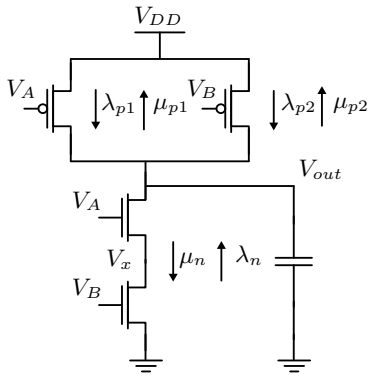

Figure 3: Poisson rates for a NAND gate, as shown in [4].

4. SIMULATOR IMPLEMENTATION

In the previous section we have derived the nodal equations used for estimating the output voltage for a logic gate. In order to take into account the nonlinear response of the circuit to noise fluctuations, we need to update the rates of the Poisson processes at each time step, before sampling the random variables X_{ch} and X_{dis}. In addition, we need to know the values of the Miller capacitances and the total output node capacitance for each gate.

A gate-level characterization of the Poisson rates and capacitances allows us to ensure accurate estimations at a minimum computational cost. For each gate we build a look-up table (LUT) which can be indexed based on the input and output voltage values. We based our characterization on a 7nm FinFET predictive technology model [17, 21]. Each gate in our library is then defined as a separate class that contains the values of the internal capacitances and the methods for reading the rate values from the matching LUT.

An abstract class representation allows us to conveniently rearrange the circuit netlist into an array of gate objects. The voltage value at each node is stored in a matrix of size

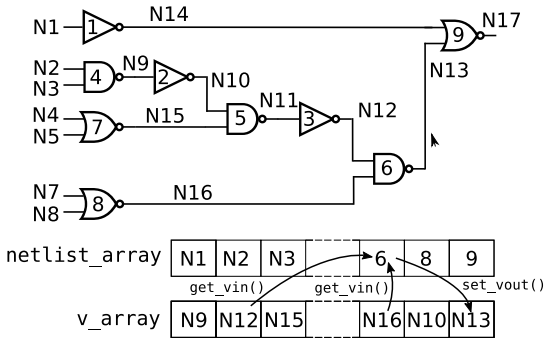

Figure 4: Mapping the circuit netlist. `get_vin()` and `set_vout()` update the gate voltages at each iteration.

$N \times$ `net_size`, where N represents the depth of the simulation buffer and `net_size` is the number of nodes in the circuit. A virtual connection between the gates is achieved by storing the appropriate indexes to the voltage matrix as input and output indexes. Figure 4 shows a simple example netlist mapped into a `netlist_array` which contains the gate instances, and a `v_array` that stores the indexed voltage values for each node. The functions `get_vin()` and `set_vout()` are used to set the biasing point for each gate. Similarly, we associate a total output capacitance of each node as the sum of its drain capacitance and the gate capacitance of every input connected to it. This initialization procedure is described in the **Init** block of Algorithm 1.

The noise generation algorithm is shown in the **Sim** block of Algorithm 1. The function `gen_noise()` computes the stochastic process for the instantaneous net electron fluctuation $X_t = X_{ch} - X_{dis}$. Since the rates for the charging and discharging components vary over time due to the change in the biasing voltages, we need to consider non-homogeneous Poisson processes (NHPP). Algorithm 2, also known as thinning [9], can be used to efficiently generate NHPP samples. This algorithm requires finding a maximizing rate $\lambda^* > \lambda(t)\ \forall t$. The samples are then generated from a distribution with rate λ^* and rejected with probability $1 - \lambda(t)/\lambda^*$. To ensure the generation of uncorrelated noise, each gate class contains two separate pseudo-random number generator engines initialized with random independent seeds.

The step-size for our simulator was fixed at 50 ps, which is below the smallest time constant extrapolated for a minimum-sized inverter using 7nm FinFETs technology operated at $V_{DD} = 180$ mV. For each gate in our netlist we update the output voltage using Equation 6. Since we need to know the output voltage of any of the fan-out stages to compute the feedback component, we split the equation between two subsequent iterations as detailed in the **Sim** block.

Data: Verilog structural netlist, gate-level parameter tables
Result: Voltage time-series
Init Parse Verilog file; Create Netlist array of gate objects
Build internal parameter LUTs
Initialize output matrix `V`
foreach $gate_i$ *in Netlist* **do**
  $gate_i(C_{out}) \longleftarrow gate_i(C_{dd})$
  foreach $gate_j$ *in Netlist* $\backslash gate_i$ **do**
    if $gate_i(O\_idx)$ *is equal to* $gate_j(I\_idx)$ **then**
      $gate_i(C_{out}) \longleftarrow gate_i(C_{out}) + gate_j(C_{gg})$
      add $gate_j$ to $gate_i(Fan\_out)$
    end
  end
  $gate_i(NoiseFactor) \longleftarrow \frac{q}{gate_i(C_{out})}$
end
Sim **while** $t < T_{end}$ **do**
  foreach $gate_i$ *in Netlist* **do**
    Update paramenters λ_t, μ_t
    forall the $gate_j$ *in* $gate_i(Fan\_out)$ **do**
      $V[t-1][gate_i(O\_idx)] =$
      $\Delta V[t-1][gate_j(O\_idx)] \times \frac{gate_j(C_M)}{gate_i(C_{tot})}$
    end
    $X_t \longleftarrow gen\_noise(\lambda_t, \mu_t)$
    $V[t][gate_i(O\_idx)] =$
    $V[t-1][gate_i(O\_idx)] + \Delta V[t][gate_i(I\_idx)] \times$
    $gate_i\left(\frac{C_M}{C_{tot}}\right) + X_t \times gate_i(NoiseFactor)$
  end
end

ALGORITHM 1: Simulator algorithm description. **Init** parses the input Verilog to create a netlist and initialize the gates' parameters. **Sim** executes the actual noise transient simulations.

Data: The current rate λ_t
Result: A sample from the NHPP for an interval of length T
$t_0 \longleftarrow 0$;
$event\_count \longleftarrow 0$;
while $t_0 < T$ **do**
  $u \longleftarrow \mathcal{U}(0,1)$;
  $v \longleftarrow \mathcal{U}(0,1)$;
  $t_0 \longleftarrow t_0 - \frac{\ln(u)}{\lambda^*}$;
  if $v < \frac{\lambda_t}{\lambda^*}$ **then**
    event_count++;
  end
end

ALGORITHM 2: Thinning algorithm for generating non–homogeneous Poisson samples.

As will be explained in Section 5, the proposed implementation allows us to speed-up noise transient simulations by at least 3 orders of magnitude when compared to SPICE-based simulations. This translates to the ability of detecting up to 5σ events in hours rather than days, where $\sigma = \sqrt{kT/C}$. However, we are interested in capturing fault inducing transients, which have amplitudes above 5σ. Therefore, we propose a methodology to reduce the simulation of thermal noise transients even further, based on the use of an incremental threshold-crossing check. At the beginning of the transient simulation we set the threshold to a value V_σ and check whether any of the circuit node voltages have fallen in the region defined by the inequality $V_\sigma < V_{out_i} < V_{DD} - V_\sigma$, indicating a departure from equilibrium logic high or low value of a node. V_σ can be arbitrarily set to the range from 0 to $V_{DD}/2$. If the desired event is reached at time t_i, we save the output traces up to the time t_j at which the voltage crosses the threshold again. At this point we re-initialize the voltage values with $V[t_0] = V[t_j]$ and increase the threshold V_σ by an arbitrary value ΔV_σ.

	# gates	# PI	# PO	This work [minutes]	SPICE [days]	speedup
rd53	63	5	3	6.1	5.6	1322x
b9	125	41	21	11.9	14.6	1766x
9sym	254	9	1	28.2	29	1480x
rd84	263	8	4	27.4	25.8	1355x
apex2	452	39	3	49.2	45	1317x
amd	629	14	24	70	68	1398x
ex5	907	8	63	101.7	92	1302x
vda	1021	17	39	162.5	126	1116x
t481	1467	16	1	291.6	133	665x
seq	2258	41	35	346	368.8	1535x

Table 1: Runtime of our simulator for MCNC benchmark circuits. The speedup is measured against the estimated runtime of SPICE running a 100 μsec noise transient simulation.

5. RESULTS

Equation 5 shows that the gate output voltage can be computed directly from the net charge fluctuations estimated by the two-sided Poisson process. In its original form, the equation cannot give us any information about the accuracy of the estimation as the computed values are random in nature. We can retrieve the equilibrium current values from the expected values of the two Poisson distribution. Without loss of generality, for the inverter in Figure 1, we have:

$$I_P - I_N = ((\lambda_p - \mu_p) - (\mu_n - \lambda_n)) \times \frac{q}{1ps}$$
$$= (\lambda_{inv} - \mu_{inv}) \times \frac{q}{1ps} = (\mathbf{E}[X_{ch}] - \mathbf{E}[X_{dis}]) \times \frac{q}{1ps}$$

As an example, we show in Figure 5 the output of a NAND gate driving an inverter from our simulator as compared to SPICE. The two traces are accurately matched for both under/overshoot and tail effects. The runtime of our simulator for a full 100 μsec simulation is compared against a SPICE transient noise analysis. For SPICE, we ran the simulation for shorter times and extrapolated a linear trend that led to the estimated runtime for a 100 μsec simulation. The simulations were run over a set of circuits from the MCNC benchmark and the results are summarized in Table 1. All circuits were simulated at $T = 100$ °C and $V_{DD} = 180$ mV. Note that this chosen value for the supply voltage is in line with other works that target noise-immune design for sub-threshold circuits [5, 8, 16]. We tested circuits with a number of gates up to 2258 and we achieved a speedup of 3 orders of magnitude.

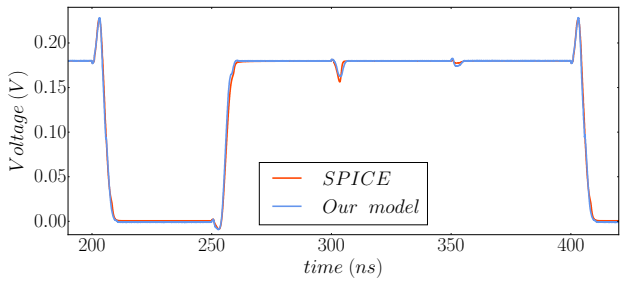

Figure 5: Output of a NAND gate as generated from our simulator and SPICE.

While our simulator can hugely improve the simulation runtime just by running a standard transient simulation, we extended its functionality using the methodology described at the end of Section 4. We set the initial threshold V_σ to 25mV and the voltage step ΔV_σ to 5 mV for $V_\sigma < 35$ mV and 2 mV otherwise. This technique could generate SET of 40 mV amplitude within few hours. The extrapolated runtime for a standard transient simulation to possibly generate the same SET would have been 10 days for our implementation, while standard SPICE could take years! We considered the possibility of running a parallel version of SPICE. However, even in an ideal situation which would allow to obtain a speedup equal to the number of available threads, it would not be possible to get to runtime values comparable to our simulator. Figure 6 shows a sample SET from our simulator. The peak amplitude is equal to 52.6 mV which is above $V_{DD}/4$.

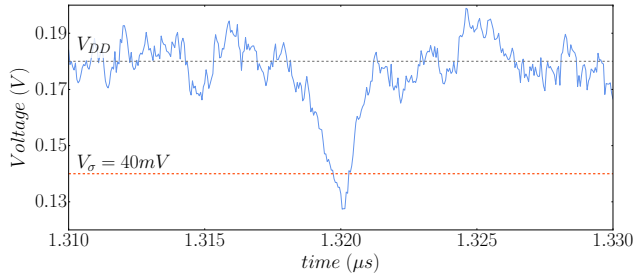

Figure 6: Example of SET generated by our simulator.

6. CONCLUSION AND FUTURE WORK

We have proposed a fast circuit simulator for the analysis of thermal noise transients in sub-threshold circuits. This tool can be used to capture rare noise-induced fault

events which would otherwise require unmanageable simulation times. Our results have shown that our implementation performs 3 orders of magnitude faster than SPICE-based simulations. Transient simulations in SPICE have shown that the runtime can be improved by taking advantage of parallelization. Our preliminary studies have shown that this is still not enough to outperform our simulator. Nonetheless, we are planning to explore multi–threaded implementation approaches that would allow to increase our performance in detecting rare transients. To the best of our knowledge, this is the first work that combines accurate modeling and fast simulation times for thermal noise transients. Additional future work will focus on using this tool for analyzing the performance of noise-tolerant circuits.

7. ACKNOWLEDGMENTS

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