Nanowire Addressing in the Face of Uncertainty

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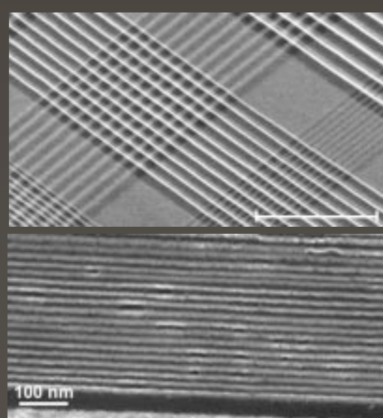
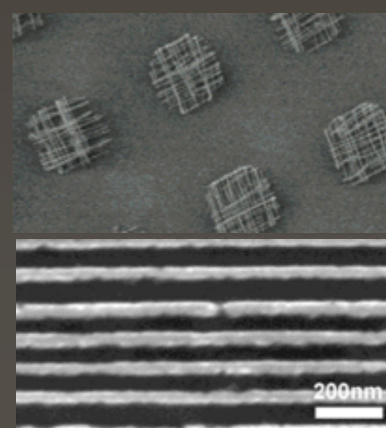
The Nanowire

- Sets of parallel NWs have been produced.
- Devices will reside at NW intersections.
- We must gain control over individual NWs.

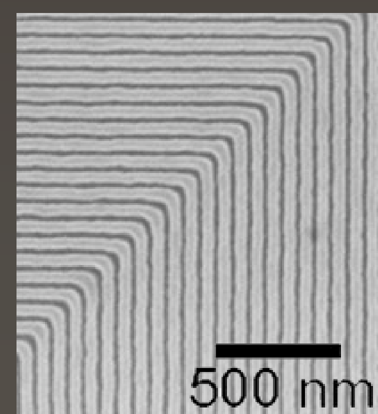
SNAP NWs
(Heath, Caltech)



CVD NWs
(Lieber, Harvard)



Directed Growth
(Stoykovich, UW)

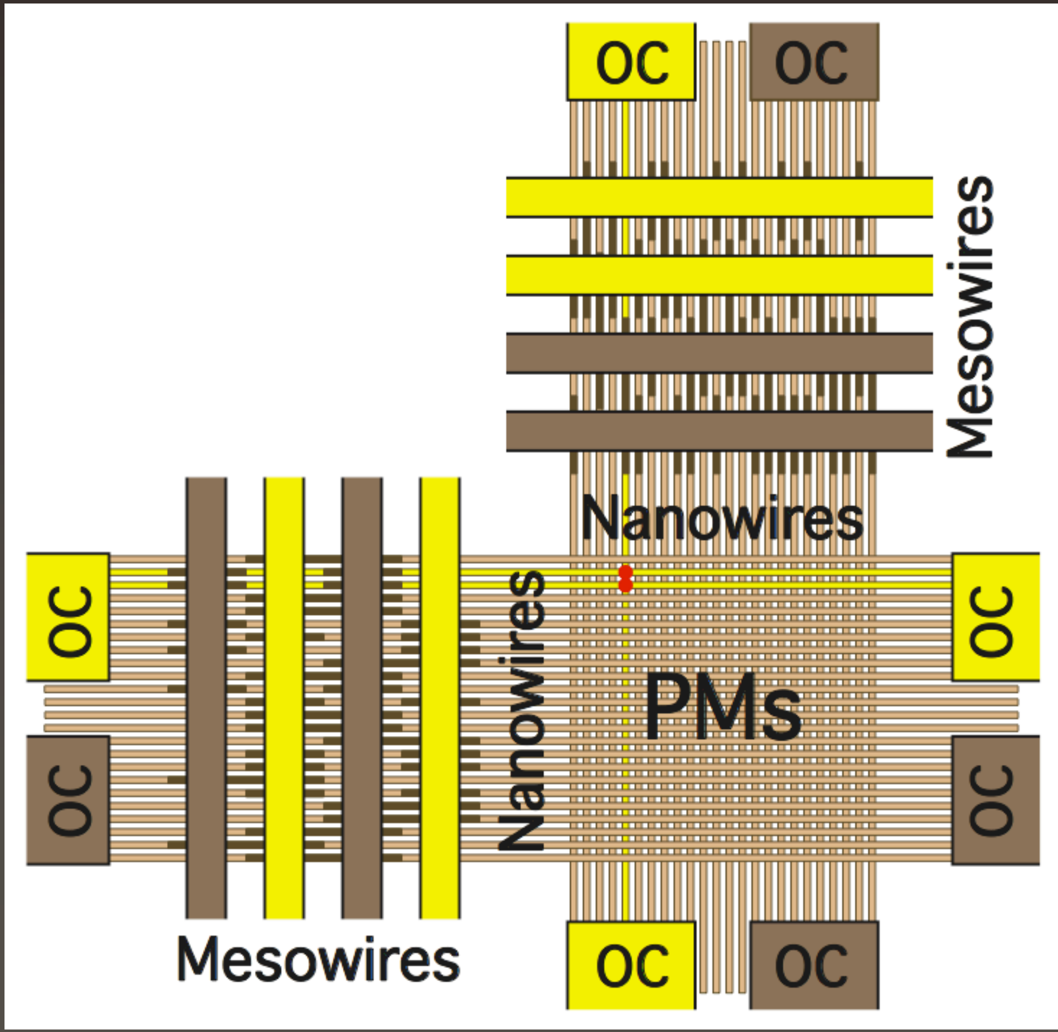


The Crossbar

The crossbar is currently the most feasible nanoscale architecture.

By addressing individual NWs, we can control programmable molecules at NW crosspoints.

Crossbars are a basis for memories and circuits.



Nanowire Control

- Mesoscale contacts apply a potential along the lengths of NWs.
- Mesoscale wires (MWs) apply fields to across NWs, some of which form FETs.
- NW/MW junctions can form FETs using a variety of technologies:

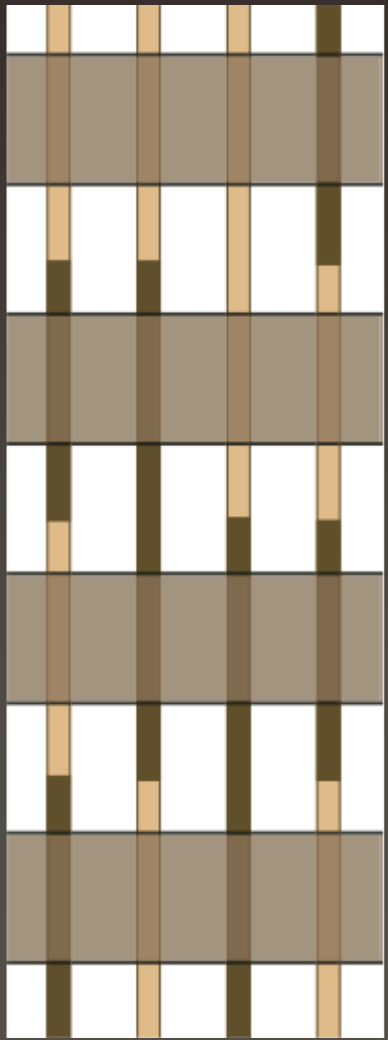
  ⇒ Modulation-doping

  ⇒ Random Particle deposition

  ⇒ Masking NWs with dielectric material

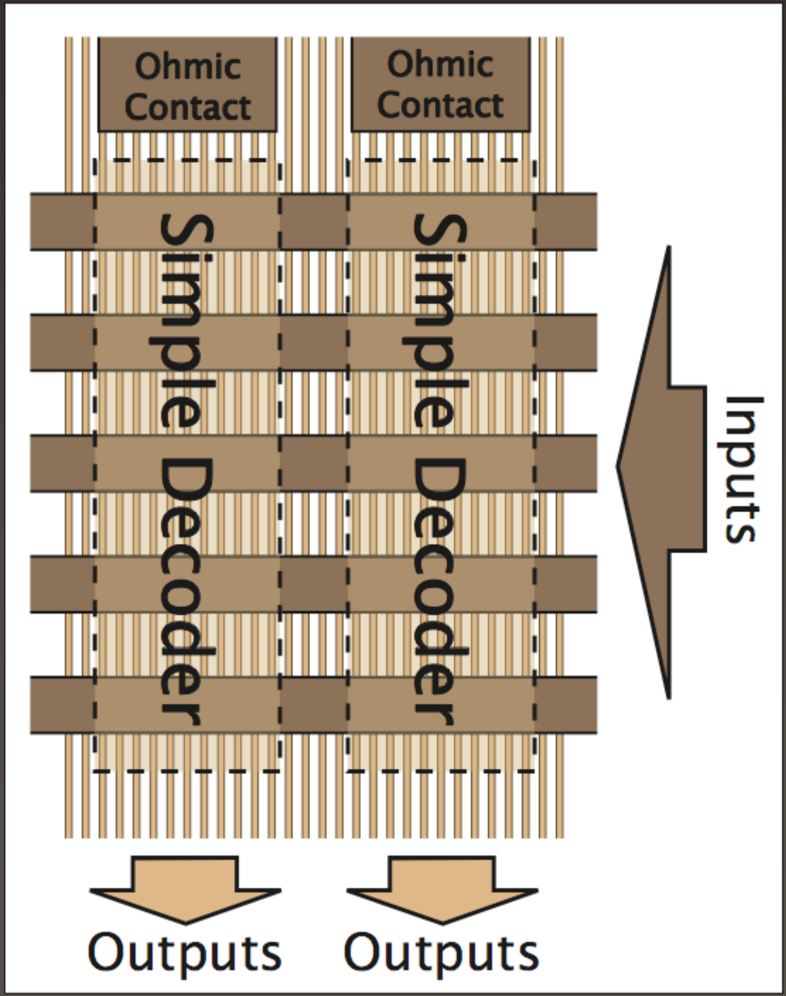
Simple NW Decoders

- A potential is applied along the NWs.
- *M* MW inputs control *N* NW outputs. Each MW controls a subset of NWs.
- When a MW produces a field, the current in each NW it controls is greatly reduced.
- Each MW “subtracts” out subsets of NWs. This permits *M* << *N*.
- Decoders are assembled stochastically and become difficult to produce as N is large.



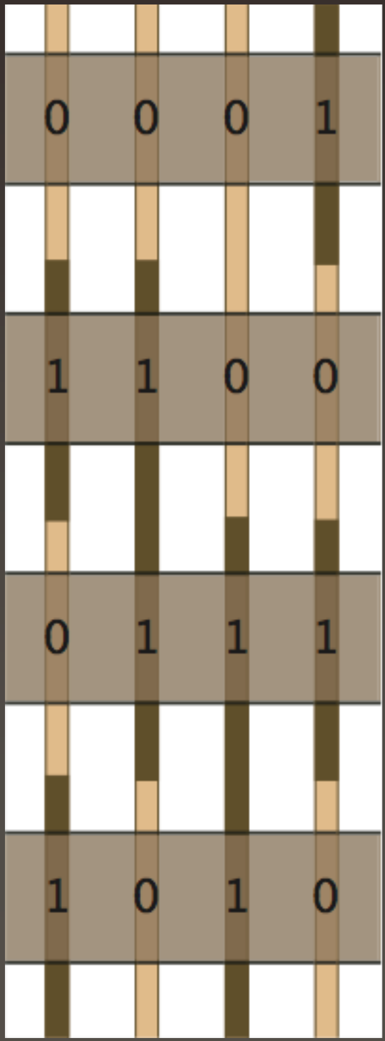
Composite Decoders

- A composite decoder uses multiple simple decoders to control many NWs.
- The simple decoders share MW inputs.
- This space savings allows for mesoscale inputs.



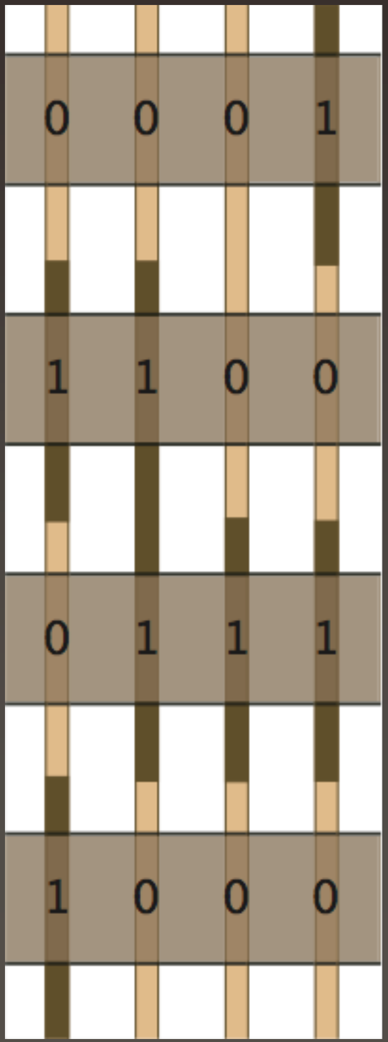
Binary Codewords

- In a NW decoder, we associate an *M*-bit codeword, c_i, with each NW, n_i.
- The jth MW controls the ith NW if and only if the jth bit of c_i, c_{ij}, is 1.
- Given the *M*-bit decoder input, *A*, n_i carries a current if and only if $A \cdot c_i = 0$.
- Codewords are assigned stochastically.
- Control over codewords is an important way to compare decoding technologies.



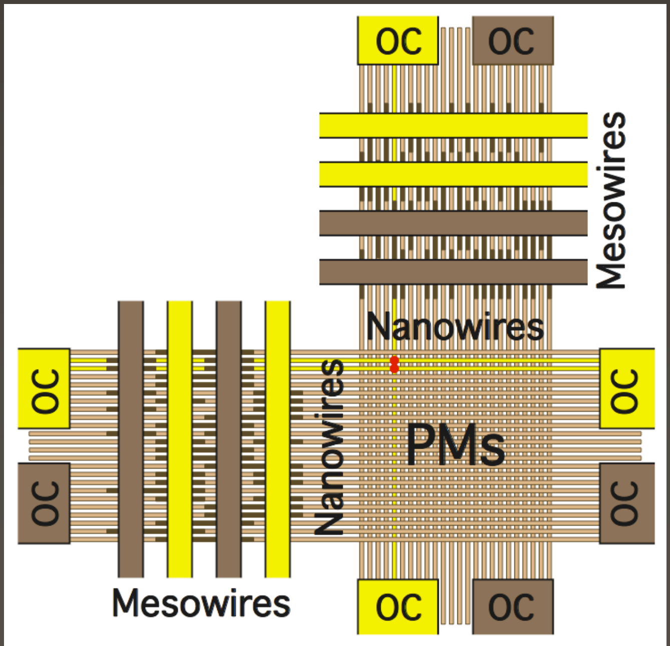
Codeword Interaction

- If $c_{bj} = 1$ where $c_{aj} = 1$, c_a **implies** c_b. Inputs that turn off n_a turn off n_b.
- A set of codewords, S, is **addressable** if some input turns off all NWs not in S.
- $S = \{c_i\}$ is addressable if and only if no codeword implies c_i. S is addressed with input $A = \overline{c_i}$.



Decoders for Memories

- A *B*-bit memory maps *B* addresses to *B* disjoint sets of storage devices.
- A ***D*-address memory decoder** addresses *D* disjoint subsets of NWs.
- Equivalently, the decoder contains *D* addressable codewords.



Decoders for Circuits

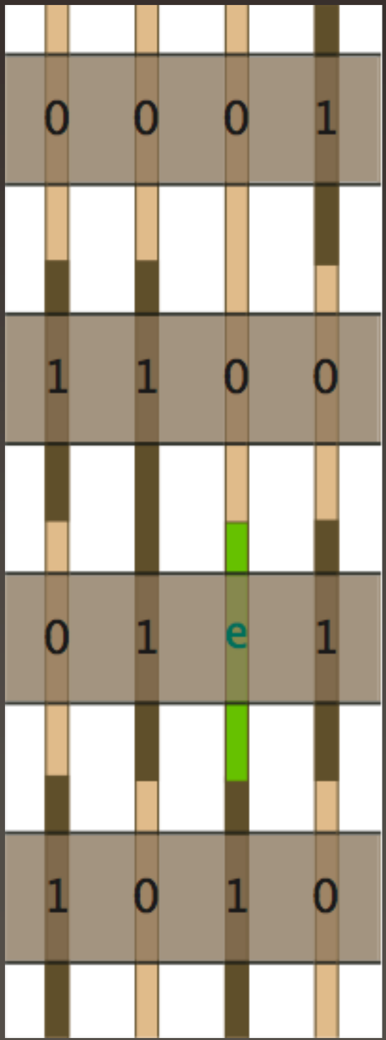
- A MW **uniquely controls** a NW if it controls only that NW.
- In a circuit with D inputs, we wish to turn on arbitrary subsets of the inputs.
- A ***D*-address circuit decoder** addresses arbitrary subsets of *D* NWs.
- Each of the D NWs must be uniquely controlled by some MW.

Imperfect Control

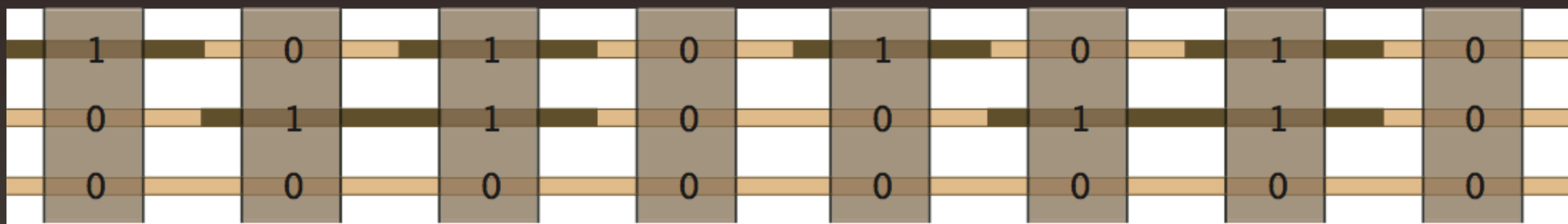
- Our binary model is accurate if each MW provides good control.
- Realistically, some MWs may only partially turn off some NWs.
- Also, some MWs may occasionally fail to control some NWs.
- Our decoders must be fault-tolerant!

Ideal Decoders with Errors

- To apply the ideal model to real-world decoders, consider binary codewords with random **errors**.
- If $c_{ij} = e$, the jth MW increases n_i's resistance by an unknown amount.
- Consider input A such that the jth MW carries a field. A functions reliably if a MW for which $c_{ik} = 1$ carries a field.



Balanced Hamming Distance



- Consider two error-free codewords, c_a and c_b. Let $|c_a - c_b]$ denote the number of inputs for which $c_{aj} = 1$ and $c_{bj} = 0$.
- The balanced Hamming distance (BHD) between c_a and c_b is $2 \cdot \min(|c_a - c_b], |c_b - c_a])$.
- If c_a and c_b have a BHD of $2d + 2$ they can collectively tolerate up to d errors.

Fault-Tolerant Random Particle Decoders

- In a particle deposition decoder, $c_{ij} = 1$ with some fixed probability, *p*.
- If each pair of codeword has a BHD of at least $2d + 2$, the decoder can tolerate *d* errors per pair.
- This holds with probability > 1- *f* when

$$M > \frac{\left(d + \left(d^2 + 4\ ln(N^2/f\,)\right)^{1/2}\right)^2}{4p(1 - p)}$$

Conclusion

- Stochastically assembled decoders can reliably control NWs even if errors occur.
- Our decoder model applies to many viable technologies. It provides conditions that a decoder must be meet.
- The requirement on circuit decoders suggests an impending IO-challenge.