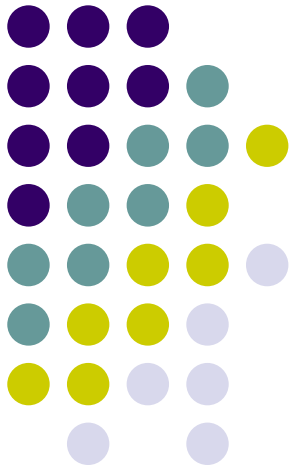
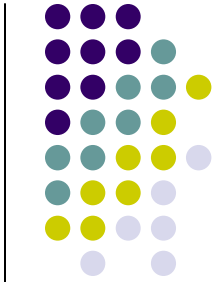
CS256
Applied Theory of Computation

VLSI Model V

John E Savage

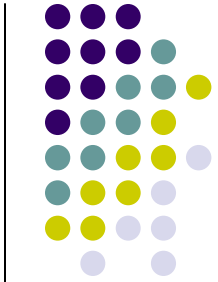


Overview



- Derivation of lower bounds on planar circuit size.
- Area-time lower bounds for functions computated by VLSI chips.

Area-Time Computational Inequalities



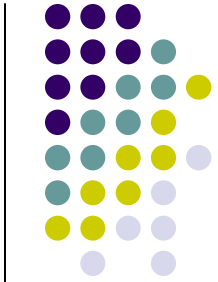
$$C_p(f) = O(min(AT^2, A^2T))$$

- To derive lower bounds on $C_p(f)$ we introduce the **planar separator theorem**. In its simplest form, it states that the vertices in every planar *n*-vertex graph can be divided into two sets with no edges between them by the removal of $O(\sqrt{n})$ vertices such that each set has between *n/3* and *2n/3* vertices.
- We use it to show that some functions have a quadratic planar circuit size in their number of inputs. The technique used is to show that a lot of information must pass from inputs to outputs.

Planar Separator Theorem

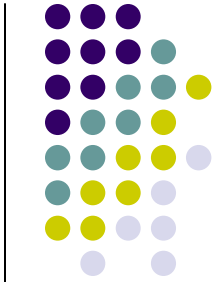
Theorem I Let G = (V,E) be an *N*-vertex planar graph having non-negative vertex costs summing to *c*(V). Then, V can be partitioned into three sets, A, B, and C, such that no edge joins vertices in A with those in B, neither A nor B has cost exceeding 2*c*(V)/3, and C contains no more than $4\sqrt{N}$ vertices.

Planar Separator Theorem



Theorem II Let G = (V,E) be an N-vertex planar graph having non-negative vertex costs summing to *c*(V). Then V can be partitioned into three sets, A, B, and C, such that no edge joins vertices in A with those in B, neither A nor B has cost exceeding 7c(V)/9, |A|, |B| ≤ 5N/6, and C contains no more than $K_1\sqrt{N}$ vertices, $K_1 = 4(\sqrt{(2/3)} + 1)$.

Planar Separator Theorem



Theorem III Let G = (V,E) be an N-vertex planar graph and let *c* be a non-negative cost function on V with total cost of *c*(V). Let P ≥ 2. There are constants $2P/3 \le q \le 3P$ and $K_2 = 4(\sqrt{(2/3)} + 1)/(1 - \sqrt{(5/6)})$ such that V can be partitioned into q sets, $A_1, A_2, \ldots, A_q$ such that for $1 \le i \le q$

$$c(V)/(3P) \le c(A_i) \le 3c(V)/(2P)$$

and sets C_i, $|C_i| \le K_2 \sqrt{N}$, and $B_i = V - A_i - C_i$ such that no edges join vertices in A_i with vertices in B_i.

Lower Bounds on Planar Circuit Size

Definition Let $f : \mathcal{A}^n \rightarrow \mathcal{A}^m$ have input variables X and outputs Y. It has a *w(u,v)*-**flow** if for all $U_1 \subseteq X$ and $V_1 \subseteq Y$ satisfying $|U_1| \geq u$ and $|V_1| \geq v$ there is a subfunction *h* of *f* from variables in U_1 to outputs in V_1 obtained by some assignment to variables in $U_0 = X - U_1$ and discarding outputs in $V_0 = Y - V_1$ such that *h* has at least $|\mathcal{A}|^{w(u,v)}$ points in the image of its domain.

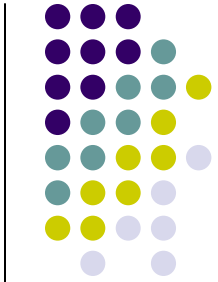
Lower Bounds on Planar Circuit Size

- We use use *w(u,v)*-flow to derive the following lower bound on the planar circuit size of a function.

  Theorem Let $f : \mathcal{A}^n \rightarrow \mathcal{A}^m$ have a *w(u,v)*-flow. Then its semellective planar circuit size must satisfy the following lower bound for $u \geq n(1-3/2P)$, $v \geq m/(3P)$, and $P \geq 2$, where $K_2 = 4(\sqrt{(2/3)} + 1)/(1 - \sqrt{(5/6)})$.

$$C_p(f) \geq w^2(u,v)/(2K_2)^2$$

Lower Bounds on Planar Circuit Size



Proof Consider a minimal semellective planar circuit for $f : \mathcal{A}^n \rightarrow \mathcal{A}^m$ on n inputs with $N = C_p(f)$ inputs, gates, & crossings. Apply Theorem III to this circuit giving unit weight to each input vertex & zero weight to all others.

Choose integer $P \leq |V|$. Then, the inputs, gates, and crossings of this circuit can be partitioned into q sets $A_1, A_2, \ldots, A_q$ for $2P/3 \leq q \leq 3P$ such that each set has $\geq n/(3P)$ and $\leq 3n/(2P)$ input vertices. Since average number of output vertices in these sets is m/q, at least one set, call it A_1, has at least the average number of output vertices, i.e. $\geq m/3P$ vertices.

Lower Bounds on Planar Circuit Size

Proof (cont.) Let U_0 and V_1 be sets of inputs and outputs in A_1, respectively. Then, $n/(3P) \le |U_0| \le 3n/(2P)$ and $|V_1| \ge m/3P$. For some assignment of values to variables in U_0, there are at least $|\mathcal{A}|^{w(u,v)}$ values for the outputs in V_1 when $u = n - |U_0| \ge n(1-3/2P)$ and $v = |V_1| \ge m/(3P)$.

Lower Bounds on Planar Circuit Size

Proof (cont.) But all of the values assumed by the outputs in V_1 must be assumed by the inputs, gates, and crossing wires of the separator. Since at most two wires cross, a separator C has at most 2|C| inputs, gates, and wires each of which can have at most $|\mathcal{A}|$ values. Thus, if C_1, the separator for A_1, has a size satisfying $2|C_1| < w(u,v)$, a contradiction results and the output variables in V_1 cannot assume $|\mathcal{A}|^{w(u,v)}$ values. It follows that $|C_1| \geq w(u,v)/2$. Since $|C_1| \leq K_2 \sqrt{N}$, we have $N \geq w^2(u,v)/(2K_2)^2$, the desired result. QED

Lower Bounds on Planar Circuit Size

Definition $f : \mathcal{A}^n \rightarrow \mathcal{A}^m$ is (α, n, m, p)-**independent** for $\alpha \geq 1$ and $p \leq m$ if it has a $w(u,v)$-flow satisfying $w(u,v) > (v/\alpha) - 1$ for all u and v satisfying $n-u+v \leq p$.

Lemma Let $f : \mathcal{A}^n \rightarrow \mathcal{A}^m$ be (α, n, m, p)-independent. For $P \geq (m/3 + 3n/2)/p$ and $P \leq m/(6\alpha)$, f has semellective planar circuit size satisfying

$$C_p \geq m^2/(144(\alpha P)^2(K_2)^2)$$

Lower Bounds on Planar Circuit Size

Proof *f* has a *w(u,v)*-flow satisfying *w(u,v)* > *(v/α) -1* for *n-u* + *v* ≤ *p*. When *u* ≥ *n*(1-3/(2P)), *n-u* + *v* ≤ *p* is satisfied if *v* ≤ *p* -*3n*/(2P). Since we also require that *v* ≥ *m*/(3P), this implies that P ≥ (*m*/3 + 3*n*/2)/p. Also, *(v/α) -1* ≥ *v*/2α if *v* ≥ 2α. Substituting *m*/3P for *v*, we have the desired conclusion. QED

Lower Bounds on Planar Circuit Size

- If f on n inputs and m outputs is (α, n, m, p)-indpndnt for $p \le m$ and $\alpha \ge 1$, there are $> |\mathcal{A}|^{(v/\alpha)} - 1$ points in the image of its domain when $\le p - v$ inputs are fixed.

Name	*Ins*	*Outs*	*Ind. Property*
Wrapped Conv	*2n*	*n*	*(2,2n,n,n/2)*
Cyclic Shift	*n+log n*	*n*	*(2,n+log n,n,n/2)*
Int Mult	*2n*	*2n*	*(2,2n,n,n/2)*
n-point FFT	*n*	*n*	*(2,n,n,n/2)*

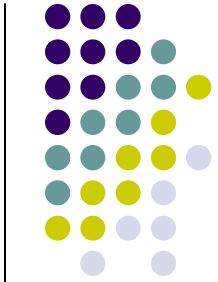
Lower Bounds on Planar Circuit Size

Lemma Let $f : \mathcal{A}^n \rightarrow \mathcal{A}^m$ be (α, n, m, p)-independent. For $P \geq (m/3 + 3n/2)/p$ and $P \leq m/(6\alpha)$, f has semellective planar circuit size satisfying

$$C_p \geq m^2/(144(\alpha P)^2(K_2)^2)$$

Lemma holds for these problems with P = 7. Lower bounds are quadratic in number of inputs.

Area-Time Lower Bounds



Theorem Area A and time T required to compute wrapped convolution and cyclic shift of n inputs, integer multiplication of n-bit integers, or the FFT on n inputs on semellective VLSI chip satisfy following:

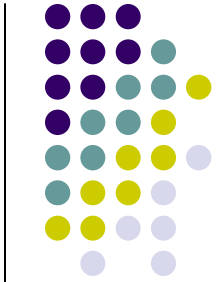
$$AT^2,\ A^2T = \Omega(n^2)$$

AT^2 lower bound can be achieved up to a constant multiplicative factor for each of these functions for $\Omega(\log n) \leq T \leq \sqrt{n}$.

Area-Time Lower Bounds

Proof Lower bound follows from circuit lower bounds. From Lect. 20, for any fully normal algorithm $AT^2 = O(n^2)$ for $\Omega(\log n) \leq T \leq \sqrt{n}$ on an embedded CCC network. Since cyclic shift and FFT are shown to be fully normal, we have matching upper and lower bounds for them. From Prob. 12.13 wrapped convolution can be realized with matching bounds on AT^2 over the same range of values for T. Same applies to integer multiplication. (Prob. 12.16.)

Comments



- The planar circuit size for cyclic shifting is $\Omega(n^2)$ but the function can be realized with $O(n \log n)$ gates.

- Since $AT^2 = \Omega(n^2)$, wires occupy more area than gates when $T = O(\sqrt{n}/\log n)$.

- Matrix multiplication lower bound requires more refined analysis.

Area-Time Bounds for Matrix Multiplication

Theorem The area A and time T required to multiply two $n \times n$ matrices with a semellective algorithm satisfies the following lower bound:

$$AT^2, A^2T = \Omega(n^4)$$

The AT^2 lower bound can be met to within a constant multiplicative factor by chip seen in Lecture 1.

Area-Time Bounds for Matrix Multiplication

Proof Apply Theorem on p. 8 to matrix multiplication by replacing the number of input variables n by $2n^2$ and the number ofoutput variables m by n^2. The $w(u,v)$-flow function has value

$$w(u,v) = (v-(2n^2-u)^2/4n^2)/2$$

$$w(u,v) \geq (n^2/2)\,(1/(3P) - (3/(2P))^2)$$

The r.h.s. is maximized when P = 14 and the coefficient of n^2 has value greater than 1/163.