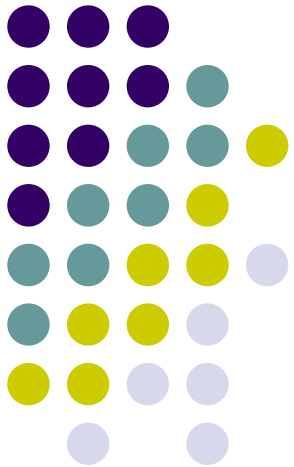
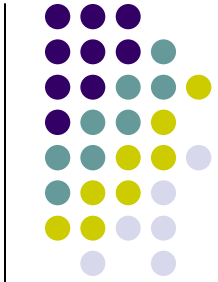
CS256
Applied Theory of Computation

VLSI Model II

John E Savage



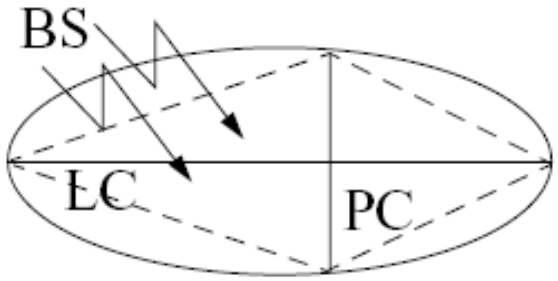
Overview



- Area-time tradeoffs – the basic idea.
- Planar circuit size.
- Two simulations of VLSI chips by planar circuits.
- Computational inequalities between area, time and planar circuit size.
- The role of the planar separator theorem.

Basic Area-Time Tradeoffs Ideas

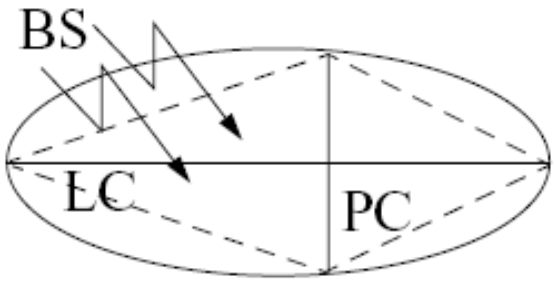
- Convex chip boundary, feature size = λ
- LC = longest chord, PC = chord ⊥ to LC divides **inputs** into two equal size sets. One side, BS, has at least half of **outputs**.



Basic Area-Time Tradeoffs Ideas

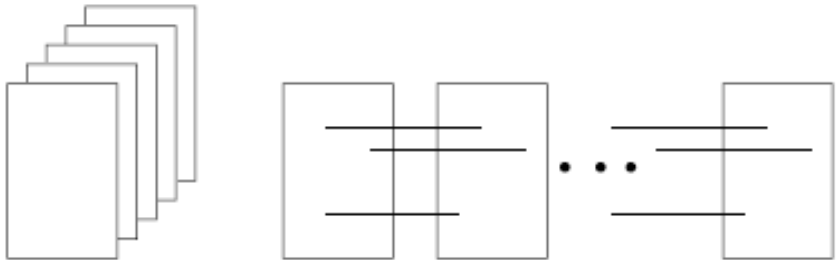
- Find bits of information, *Inf*, that must move to outputs in BS from inputs on other side.
- At most |PC|/2λ wires cross PC.
- Number of steps T ≥ *Inf* / (|PC|/2λ).
- Area A ≥ |PC||LC|/2 ≥|PC|^2/2. Thus,

$$AT^2 \geq 2\lambda^2 \, Inf^{\,2}$$



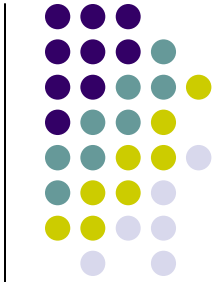
Our Approach – Via Planar Circuits

- We simulate T steps by a chip (an FSM) by two planar circuits.



- First has planar circuit of size $O(AT^2)$. Second has size $O(A^2T)$.

Planar Circuit Size



Definition A **planar circuit** over set a X is a circuit over X embedded in the plane in such a way that gates do not overlap but edges may cross.

The **size** of a planar circuit is the number of inputs, edge crossings, and gates drawn in a planar circuit in which gates realize functions over X.

The **planar circuit size** of a function $f : X^n \rightarrow X^m$, $C_p(f)$ (when the basis is understood) is the size of the smallest planar circuit for f over the given basis.

A planar circuit is **semellective** if there is a unique vertex at which each input variable is supplied. Otherwise it is **multilective**.

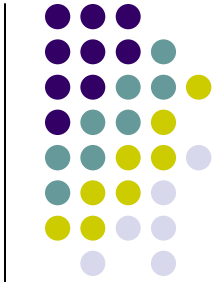
Our Approach – Via Planar Circuits

- The size of the smallest planar circuit, $C_p(f)$, for a function f computed by chip of area A in T steps is no larger than either bound. That is

$$C_p(f) = O(A^2T) \text{ and } C_p(f) = O(AT^2)$$

- We use the **planar separator theorem** to derive lower bounds on the planar circuit size, $C_p(f)$, of the function f. If $C_p(f)$ is large, so are both A^2T and AT^2.

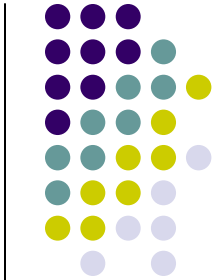
Planar Circuit Size



Lemma The planar circuit size $C_p(f)$ and standard circuit size $C(f)$ of $f : B^n \rightarrow B^m$ over a basis Ω are related as follows where r is the fan-in of Ω.

$$C(f) + n \leq C_p(f) \leq (rC(f))^2/2 + C(f) + n$$

Planar Circuit Size

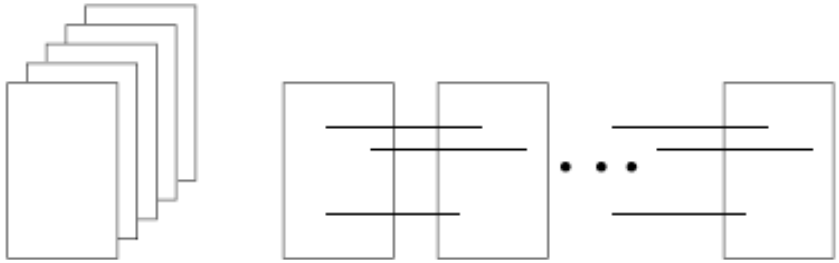


$$C(f) + n \le C_p(f) \le (rC(f))^2/2 + C(f) + n$$

Proof The first inequality is obvious. The second is straight-forward to obtain. Note that there are at most $rC(f)$ wires connecting inputs and gates to other gates. Consider any planar embedding of a minimal circuit for f (containing $C(f)$) gates. It isn't necessary for two wires to cross more than once; if they do, swap their respective segments. Since there are at most $q(q-1)/2$ pairs of elements from a set of q elements, it follows that there are $\le (rC(f))^2/2$ crossings from which the result follows. QED

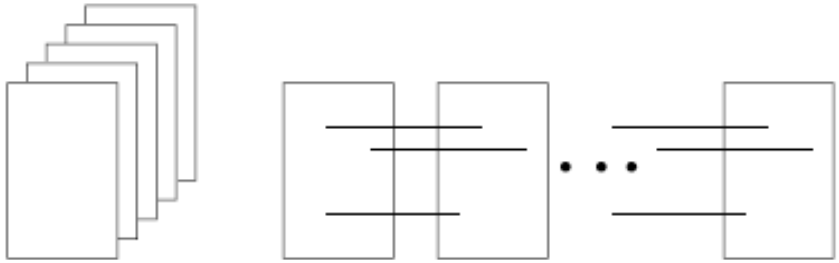
- In section 12.7 of *Models of Computation* we show cyclic shifting function nearly meets upper bound.

First Computational Inequality



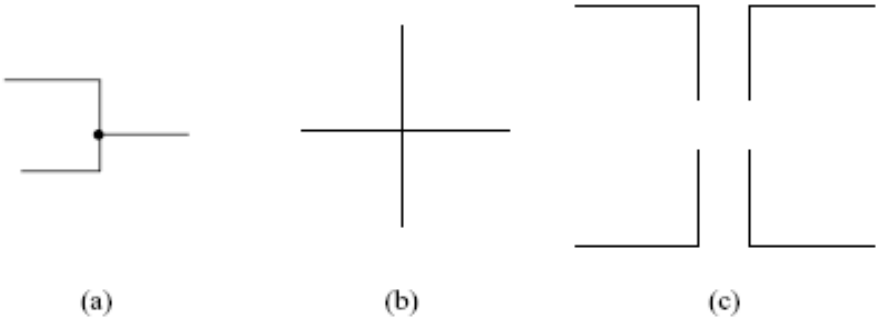
- We use simulation to show $C_p(f)=O(min(AT^2,A^2T))$
- To show $C_p(f) = O(AT^2)$, stack T copies of chip one above the other; replace each memory cell by a wire and pass a wire from its output on one stack to its input on the next. Produce a planar circuit by shrinking all inputs, wires, and gates to zero width.

First Computational Inequality



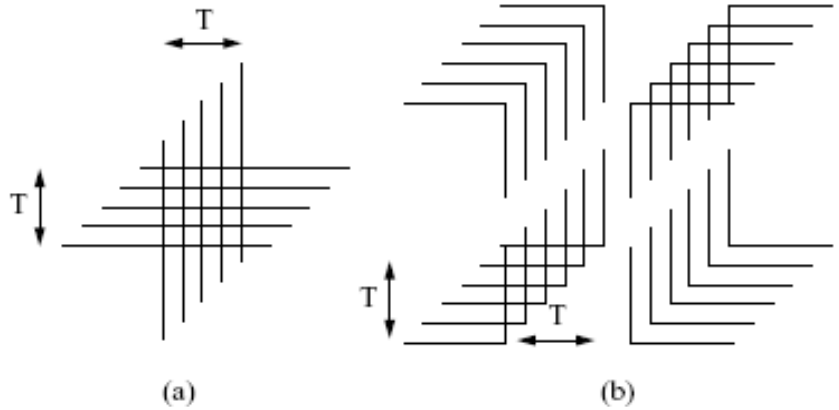
- Displace T copies of the chip infinitessimally from one another to the northeast. When seen from above, this exposes crossing (rectilinear) wires as well as individual gates and inputs. The number of gates and inputs is T times the number on one chip. How many crossing wires result from displacement?

First Computational Inequality



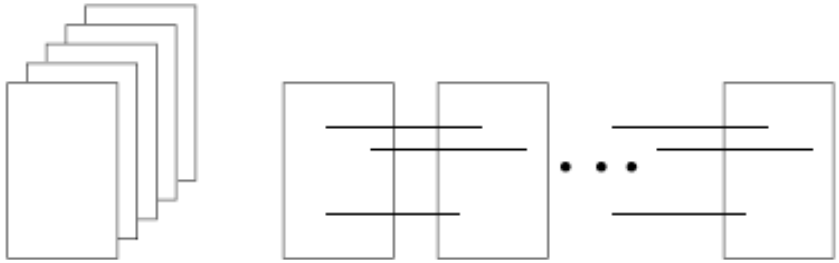
- Shown in a) is effect of gate shrinkage. b) shows crossing wires, and c) shows four ways wires meet.

First Computational Inequality



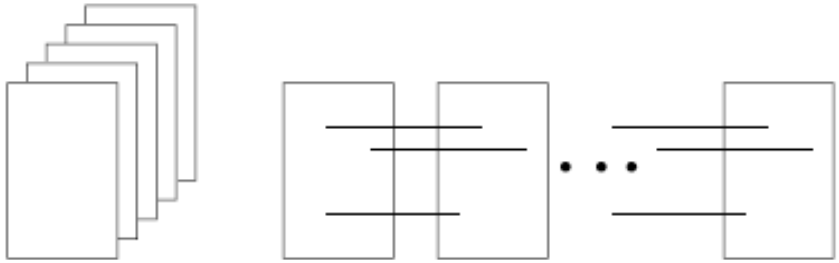
- The effect of the displacement on crossing wires is shown in a) and on wires that meet in b). Maximum number of crossings resulting from meeting or crossing wires is $O(T^2)$. Number of crossings or meetings on chip is at most A/λ^2. Thus, the size of planar circuit in this construction is $O(AT^2/\lambda^2)$.

Second Computational Inequality



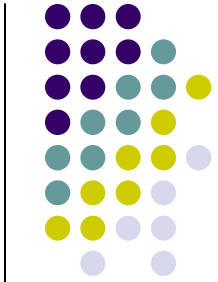
- To show $C_p(f) = O(A^2T)$ place copies of chip side by side, replace memory cells by wires, and make wires and gates infinitessimal.

Second Computational Inequality



- To make connections between copies of the chip, we vertically stretch each chip enough to pass wires from memory cell outputs on one chip to inputs on another. Since a wire from a cell (of which there are $n_W \leq A/\lambda^2$) may cross every wire in the original circuit, the number of crossings in one copy of the chip is increased from the original value (at most A/λ^2) by at most n_W^2. Thus, the number of crossings and gates is at most $O(AT + A^2T) = O(A^2T)$.

Area-Time Computational Inequalities



$$C_p(f) = O(min(AT^2, A^2T))$$

- To derive lower bounds on $C_p(f)$ we introduce the **planar separator theorem**. In its simplest form, it states that the vertices in every planar *n*-vertex graph can be divided into two sets with no edges between them by the removal of $O(\sqrt{n})$ vertices such that each set has between *n/3* and *2n/3* vertices.
- We will use it to show that some functions have a quadratic planar circuit size in their number of inputs. The technique used is to show that a lot of information must pass from inputs to outputs.